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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
DOTY, HEATHER ANNE

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,345	WU, SHYH-ING	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-21 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 13-21 and 23 are objected to because of the following informalities: Claim 13 (lines 13-14) contains the limitation "wherein the first under-bump-metallurgy layer remains covering on the active surface of the wafer," which is not clear language. The examiner assumes that the first under-bump-metallurgy layer remains covering the active surface of the wafer. Appropriate correction is required. Claims 14-21 and 23 are objected to for depending from claim 13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7, 9, 10, 13-16, 18, 19, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) in view of Lu et al. (U.S. 6,440,836).

Regarding claim 1, APA teaches a process for forming a plurality of bumps on a wafer with an active surface, wherein the wafer further includes a passivation layer, a polymer layer and a plurality of bonding pads over the active surface, and the bonding pads are exposed by a plurality of first openings in the passivation layer and the polymer layer (instant specification paragraph 0007), the process comprising the steps of:

--forming an adhesion layer over the active surface of the wafer covering the bonding pads and the polymer layer (instant specification paragraph 0008);

--forming a barrier layer on the adhesion layer (instant specification paragraph 0008);

--forming a wettable layer on the barrier layer (instant specification paragraph 0008);

--removing a portion of the wettable layer and a portion of the barrier layer such that the residual wettable layer and the residual barrier layer remain on the bonding pads (instant specification paragraph 0009 and Fig. 1C);

--forming a patterned mask layer, wherein the mask layer has a plurality of second openings that at least exposes the wettable layer (instant specification paragraph 0010 and Fig. 1D);

--performing a printing process to form a solder paste layer including solder powders and a flux (instant specification paragraph 0014) inside the second openings by depositing solder paste into each second opening (instant specification paragraph 0011 and Fig. 1E);

--performing a first reflow process to transform the solder paste layer inside each second opening into a bump (instant specification paragraph 0012 and Fig. 1F); and

--removing the patterned mask layer (instant specification paragraph 0013).

APA does not teach that the step of forming the patterned mask layer includes forming the mask layer on the adhesion layer, that the solder paste layer contacts the

adhesion layer but not contacts the polymer layer, or removing the adhesion layer outside the residual wettable and the residual barrier layer.

Lu et al. teaches a method of forming a plurality of bumps on a wafer, the process comprising the steps of forming an adhesion layer (column 7, line 54 – column 8, line 6; **82** in Fig. 3B), a barrier layer (**84** in Fig. 3B), and a wettable layer (not labeled, but considered part of BLM layer **80** in Fig. 3B; column 7, line 67 – column 8, line 1), removing a portion of the wettable layer and a portion of the barrier layer (Fig. 3D shows upper levels of the BLM layer removed from the regions not on the contact pad **72**), forming a patterned mask layer (**100** in Fig. 3G) on the adhesion layer, and removing the adhesion layer outside the residual wettable and the residual barrier layer (Fig. 3I). Lu et al. teaches that this method enables an improved process for fabricating fine-pitched solder balls on any suitable electronic substrate (column 9, lines 19-22). Additionally, although Lu et al. does not teach the presence of a polymer layer, Lu et al. clearly teaches that the only layer the solder contacts is the barrier layer, **84** in Fig. 3H.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the bump-forming method taught by APA by removing portions of the wettable and barrier layers only, and then forming the patterned mask layer over the adhesion layer, as shown in Figs. 3D-3G of Lu et al., and after forming the solder layer, removing the remaining adhesive layer not under the solder, as shown in Fig. 3I of Lu et al. Moreover, as combined with APA, the solder layer would not contact the polymer layer because the adhesion layer (taught by both APA and Lu et al.) remains under the photoresist layer, as taught by Lu et al. The motivation for doing

so at the time of the invention would have been that the method taught by Lu et al. enables an improved process for fabricating fine-pitched solder balls on any suitable electronic substrate.

Regarding claim 2, APA and Lu et al. together teach the process of claim 1. APA further teaches performing a second reflow process to treat the bumps (instant specification paragraph 0013).

Regarding claims 3 and 7, APA is silent regarding the material composition of the adhesion and wettable layers. However, Lu et al. teaches that the adhesion layer is comprised of aluminum and the wettable layer of copper (column 7, lines 34-39). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a bump using the method taught by APA and Lu et al. together, and taught by claim 1, and further make the adhesion layer of aluminum and the wettable layer of copper. The motivation for doing so at the time of the invention would have been that these are normal materials for such applications, as taught by Lu et al. (column 2, lines 28-30) and using them would save the time and resources involved in developing alternative materials.

Regarding claim 9, APA and Lu et al. together teach the process of claim 1. APA is silent regarding the composition of the bonding pads, but Lu et al. teaches that the bonding pads are made of aluminum (column 2, lines 12-14). Therefore, at the time of the invention, it would have been obvious for one of ordinary skill in the art to form a bump using the process taught by APA and Lu et al. together, and also taught by claim 1, and form the bonding pads of aluminum because it is a conductive metal, and a

conventional material for such an application, as taught by Lu et al. (column 2, lines 8-14).

Regarding claim 10, APA and Lu et al. together teach the process of claim 1. Lu et al. further teaches that the bonding pads are made of aluminum (see rejection of claim 9 above) and that the under-bump-metallurgy is an aluminum/nickel-vanadium alloy/copper composite layer (see rejection of claims 3, 6, and 7 above).

Regarding claim 13, APA teaches a process of fabricating bumps on an active surface of a wafer, comprising the steps of:

--forming a first under-bump-metallurgy layer on the active surface of the wafer (instant specification, paragraph 0008);

--forming a second under-bump-metallurgy layer on the first under-bump-metallurgy layer (instant specification, paragraph 0008);

--removing a portion of the second under-bump-metallurgy layer (instant specification, paragraph 0009);

--forming a patterned mask layer, wherein the mask layer has a plurality of openings that at least exposes the second under-bump-metallurgy layer (instant specification, paragraph 0012);

--performing a printing process to deposit a solder paste layer into the openings, wherein the solder paste layer is made of a mixture including solder powders and a flux (instant specification, paragraph 0014);

--performing a first reflow process to transform the solder paste layer inside the openings into bumps, wherein the first under-bump-metallurgy layer remains covering

the active surface of the wafer (instant specification, paragraph 12—the claim preamble recites a process of fabricating bumps on an active surface of a wafer, so the active surface includes the portion under the solder paste layer) ; and

--performing a second reflow process to treat the bumps (see instant specification paragraphs 0008-0013).

APA does not teach that forming the patterned mask layer includes forming the patterned mask layer over the first under-bump-metallurgy layer, or removing the first under-bump-metallurgy layer outside the residual second under-bump-metallurgy layer.

Lu et al. teaches a method of forming a plurality of bumps on a wafer, the process comprising the steps of forming a first under-bump-metallurgy layer (adhesion layer, column 7, line 54 – column 8, line 6; **82** in Fig. 3B), a second under-bump-metallurgy layer (**84** in Fig. 3B; column 7, line 67 – column 8, line 1), removing a portion of the second under-bump-metallurgy layer (Fig. 3D shows upper levels of the BLM layer removed from the regions not on the contact pad **72**), forming a patterned mask layer (**100** in Fig. 3G) over the adhesion layer, and removing the adhesion layer outside the residual wettable and the residual barrier layer (Fig. 3I). Lu et al. teaches that this method enables an improved process for fabricating fine-pitched solder balls on any suitable electronic substrate (column 9, lines 19-22).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the bump-forming method taught by APA by removing portions of the second under-bump-metallurgy layer only, and then forming the patterned mask layer over the adhesion layer, as shown in Figs. 3D-3G of Lu et al., and

after forming the solder layer, removing the remaining adhesive layer not under the solder, as shown in Fig. 3I of Lu et al. The motivation for doing so at the time of the invention would have been that the method taught by Lu et al. enables an improved process for fabricating fine-pitched solder balls on any suitable electronic substrate.

Regarding claims 14 and 18, APA and Lu et al. together teach the process of claim 13. APA further teaches that the second under-bump-metallurgy layer at least comprises a wettable layer and an adhesion layer (instant specification paragraph 0008).

Regarding claims 15 and 19, APA and Lu et al. together teach the process of claim 13. APA is silent regarding the material composition of the wettable and adhesion layers, but Lu et al. teaches that a material of the wettable layer comprises copper and the adhesion layer is made of titanium (column 2, lines 28-30; column 7, lines 37-38; column 8, lines 1-3). Therefore, at the time of the invention, it would have been obvious to form a bump using the process taught by APA and Lu et al. together, and also taught by claim 13, and further make the wettable layer from copper. The motivation for doing so at the time of the invention would have been that these are normal materials for such applications, as taught by Lu et al. (column 2, lines 28-30) and using them would save the time and resources involved in developing alternative materials.

Regarding claim 16, APA and Lu et al. together teach the process of claim 14. APA further teaches that the step of forming a second under-bump-metallurgy layer on the first under-bump-metallurgy layer further includes the steps of forming a barrier layer

on the first under-bump-metallurgy layer and forming the wettable layer on the barrier layer (instant specification paragraph 0008).

Regarding claim 23, APA and Lu et al. together teach the process of claim 13. APA further teaches that the wafer includes a polymer layer disposed over the active surface, and the first under-bump-metallurgy layer disposed on the polymer layer (polymer layer **108**, under-bump-metallurgy layers **112** in Fig. 1B).

Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) in view of Lu et al. (U.S. 6,440,836) and Cronin et al. (U.S. 6,140,703).

Regarding claims 6 and 17, APA and Lu et al. together teach the process of claims 1 and 16. APA is silent regarding the composition of the barrier layer, but Lu et al. teaches that a material of the barrier layer includes nickel-vanadium alloy (column 7, line 38). Therefore, at the time of the invention, it would have been obvious to form a bump using the process taught by APA and Lu et al. together, and also taught by claim 16, and further make the barrier layer from a nickel-vanadium alloy. The motivation for doing so at the time of the invention would have been because a composition of nickel and vanadium forms a barrier that inhibits the dissolution of nickel and its subsequent diffusion during solder reflow processes, as expressly taught by Cronin et al. (column 2, lines 54-56).

Claims 4, 5, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) in view of Lu et al (U.S. 6,440,836) and further in view of Agarwala (U.S. 5,376,584).

Regarding claims 4, 5, 20, and 21, APA and Lu et al. together teach the processes of claims 1 and 19. They do not teach that the step of removing the adhesion layer comprises using an etching solution for etching the adhesion layer, wherein the etching solution does not react with the bumps.

Agarwala teaches a method of forming a bump that comprises etching an adhesion layer after the bump is formed using an etch solution that does not react with the bump (column 4, lines 33-38; since the solder bump is reflowed after the chemical etch, it is inherent that the etch did not react with the bump).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by APA and Lu et al. together, and also taught by claims 1 and 19, and further remove the adhesion layer using an etch solution that does not react with the bumps. The motivation for doing so at the time of the invention would have been to protect the bumps for future processing steps such as reflow, as taught by Agarwala et al. (column 4, lines 37-38).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) in view of Lu et al. (U.S. 6,440,836) as applied to claim 1 above, and further in view of Kim et al. (U.S. 6,417,089).

Regarding claim 8, APA and Lu et al. together teach the method of claim 1, but do not teach that the polymer layer is made of a material selected from the group consisting of benzocyclobutene and polyimide.

Kim et al. teaches forming an insulation layer above a passivation layer and beneath an under-bump-metallurgy layer wherein the insulation layer comprises a

polymer selected from the group consisting of benzocyclobutene and polyimide (column 3, lines 26-35). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a bump according to the method taught by APA and Lu et al. together, and also taught by claim 1, and further make the polymer layer from benzocyclobutene or polyimide, since it is known in the art to do so, as taught by Kim et al. Further, it has been held that the selection of a known material based on its suitability for its intended use supports a prima facie obviousness determination (*Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945)).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) in view of Lu et al. (U.S. 6,440,836) as applied to claim 11 above, and further in view of Higdon et al. (U.S. 6,375,062).

Regarding claim 11, APA and Lu et al. together teach the process of claim 9, but do not teach that the under-bump-metallurgy is a titanium/nickel-vanadium alloy/copper composite layer when the bonding pads are made of copper.

Higdon et al. teaches a solder bumping method that uses copper bonding pads wherein it is particularly suitable to use a titanium/nickel-vanadium alloy/copper composite layer for the under-bump-metallurgy layer (column 4, lines 34-38 and 54-58). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a solder bump according to the process taught by APA and Lu et al. together, and also taught by claim 9, and further make the bonding pads of copper and the under-bump-metallurgy of titanium/nickel-vanadium alloy/copper composite. The motivation for doing so at the time of the invention would have been that Higdon et

al. teaches that this under-bump-metallurgy layer is particularly suitable in bump-forming processes. Further, it has been held that the selection of a known material based on its suitability for its intended use supports a prima facie obviousness determination (*Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945)).

Response to Arguments

Applicant's arguments filed 6/30/2006 have been fully considered but they are not persuasive.

On page 9 of the Remarks, Applicant argues that Lu fails to disclose that the reflow process is performed while the adhesion layer 82 still remains. However, Applicant does not claim this limitation. In the last five lines of claim 1, Applicant recites "performing a first reflow process to transport the solder paste layer inside each second opening into a bump; removing the patterned mask layer; and removing the adhesion layer outside the residual wettable and the residual barrier layer." Applicant does not claim an order for these method steps or that the reflow process is performed while the adhesion layer remains.

Applicant further argues that "Lu never considers the situation when the polymer layer is further formed on the passivation layer 76 at all, therefore Lu apparently does not equally disclose the claimed features" (second paragraph under heading 2). In the same paragraph, Applicant continues to argue that the etching process is performed to remove the photoresist layer with layers 82 and 96 without specific consideration of the damage that could be caused to the wafer, which "may even have the polymer layer."

These arguments appear to contradict each other, regarding the presence of the polymer layer. Applicant initially argues that Lu et al. does not teach the presence of a polymer layer, and then admits that the wafer may contain a polymer layer. As best understood by the examiner, Applicant's argument is that Lu et al. does not expressly teach the presence of the polymer layer, so does not disclose the claimed features, and even if Lu et al. did teach that the wafer included a polymer layer, Lu et al. does not take into consideration the safety of this layer while etching the photoresist layer with layers 82 and 96, as in Fig. 3I.

The first of these arguments is not persuasive because it is the examiner's position that the combination of APA and Lu et al. teach the claimed features, not Lu et al. alone. APA teaches the polymer layer and Lu et al. teaches leaving the adhesion layer on the wafer under the photoresist layer (reading on the claim 1 limitation "forming a patterned mask layer on the adhesion layer") while solder is deposited (Fig. 3H). The second argument is also not persuasive because Lu et al. need not consider potential damage to the wafer in order for the combination of APA and Lu et al. to read on claim 1. Claim 1 does not include the limitation that the polymer layer is in any way protected while the mask pattern is removed.

In the last paragraph on page 9, Applicant argues that solder bump 120 taught by Lu et al. is provided by an electroplating process, and not a printing process. However, the examiner relies on APA for the teaching of a printing process, and never states that Lu et al. teaches a printing process.

On page 10, first full paragraph, Applicant argues that the adhesion layer 82 taught by Lu "is not used with the function to protect the polymer layer of the present invention from being etched and therefore does not equal to the adhesion layer of the present invention."

This argument is not persuasive because regardless of the intended use of the adhesion layer taught by Lu et al., it is clearly still an adhesion layer, and Lu et al. does teach forming a patterned mask layer on this adhesion layer, as required by claim 1.

Applicant finally argues that Lu teaches that the two steps of solder reflow and adhesion layer etching may be reversed, and that this is different from the present invention because the adhesion layer has been removed before the step of solder reflow. However, as stated above, neither claim 1 nor claim 13 recites any limitation about the order of the method steps. Claim 13 includes the limitation that the first under-bump-metallurgy layer remains covering the active surface of the wafer during the first reflow process, but this language is not specific, since the active surface of the wafer includes the portion where the bump is formed, which is covered by the first under-bump-metallurgy layer (Fig. 1).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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